A 5.8 GHz 1.77mW AFSK-OFDM CMOS Backscatter Transmitter for Low Power Internet of Things Applications

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***Abstract* — This paper presents an AFSK-OFDM (amplitude frequency shift keying-orthogonal frequency division multiplexing) based backscatter transmitter for Internet-of-Things (IoT) applications. The transmitter uses an array of 4 low-power direct digital frequency synthesizers (DDFSs) and DACs to transmit data using both frequency and amplitude symbols on 4 different OFDM subcarriers. The backscatter modulator is demonstrated within a 5.8 GHz wireless link using an 8-symbol OFDM library at a range of 2.7m and shown to consume 1.77 mW when operated at a symbol rate of 4MS/s (corresponds to 12 Mb/s). The modulator chip occupies 0.45mm² of silicon area.**

Index Terms — Backscatter modulator, OFDM, ASK.

I. Introduction

In the last 10 years, orthogonal frequency division multiplexing (OFDM) has rapidly become the modulation used for almost all 802.11 WLAN standards and almost all of the 3G/WCDMA and 4G LTE wireless standards. The reasons for this are obvious, OFDM offers high robustness to fading and dynamic channel conditions, as well as high spectral efficiency. While link performance remains high, the major drawback of OFDM is that its implementation is fairly complicated compared with single-carrier schemes. As shown in Fig. 1, OFDM is typically implemented using an IFFT:FFT pair within the transmitter and receiver. Symbol representation is accomplished where multiple sub-carriers (each bin of the FFT) are each given a phase and amplitude during each symbol period. The entire sequence of symbols is transformed to a time-domain signal by an IFFT and streamed out a DAC to the RF transmitter and channel. At the receiver the captured time-domain signal is then transformed back to frequency domain by an FFT and the amplitude-phase pairs of each sub-carrier are identified to decode the transmitted symbol.

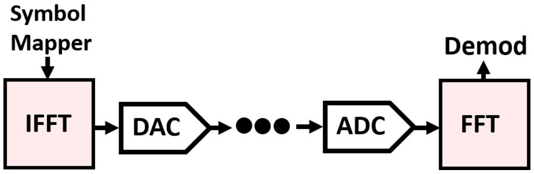

Fig. 1. Traditional OFDM modulation system where an IFFT and FFT are used to translate between frequency-domain for symbol generation and identification, and time-domain for transmission/reception.

As the IFFT processor consumes large power in the transmitter [1] this approach to OFDM is difficult for IoT devices where extremely low power data links are required. One extremely common approach for IoT is backscatter communication, an approach similar to RFID where a base-station illuminates a tag or device and it modulates its own reflection coefficient to relay data to a receiver co-located at the base-station. Many excellent demonstrations of backscattering have been performed with single carrier modulations of ASK[2], QPSK[3] and even 16 QAM[4]. However the IFFT required for the transmitter has remained prohibitive in allowing backscattering to use OFDM schemes.

II. AFSK-OFDM Backscatter modulator

In order to provide OFDM modulations in a backscattered link we have developed an AFSK-OFDM (amplitude frequency shift keying-orthogonal frequency division multiplexing) based backscatter transmitter which uses DDFS circuitry instead of an IFFT to generate the required time-domain signal for transmission. AFSK-OFDM originates from the bell telephone system where each stage and command is represented by a set of several tones or sub-carriers, each at specific frequencies and amplitudes. Hence the name of key telephone features "dial-tone", "call-tone" and "touch-tone dialing". More recently AFSK-OFDM was used in telephone computer modems with the symbols often in audible frequency range leading to the famous dial-up modem noises "dee, doo, bzzzzzzzz" (remember AOL?…right before the "you've got mail!" part). In our backscatter transmitter we use this same AFSK modulation where each transmitted data symbol is represented by up to 4 simultaneous tones (each with a specific frequency and amplitude).

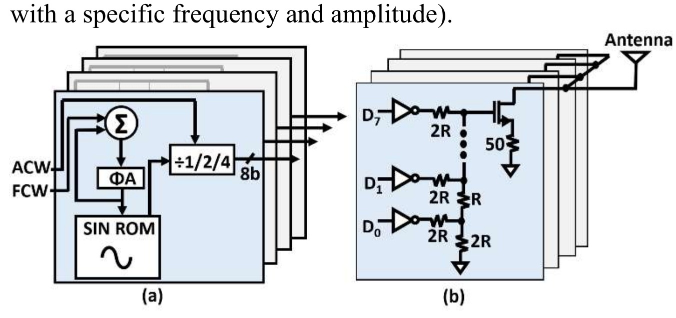

Fig. 2.(a) DDFS portion of our AFSK-OFDM backscatter transmiter. (b) R2R DAC and RF modulator section showing circuit schematic (R=20K ohm).

Figure 2a shows the implementation of our AFSK-OFDM backscatter generator. Four parallel direct digital frequency synthesizers (DDFSs) generate up to 4 tones using a digital phase accumulator and sin rom which converts phase to voltage. Each DDFS receives a 2-bit amplitude control word (ACW) and 5-bit frequency control word (FCW) allowing it to produce a unique amplitude/phase tone. Each DDFS is clocked at 32 MHz with its 5 bit FCW allowing a sub-carrier anywhere from 0-16 MHz with 0.5 MHz step size to be produced. Depending on the ACW the output of each DDFS is scaled with fixed factors of 0, 1, 2, or 4 to produce different amplitudes. Considering the 4 parallel DDFS sub-carrier paths, the 4 possible amplitudes and 32 possible frequencies, exactly 4x4x32 = 512 different potential symbols can be generated by this AFSK-OFDM modulator. More sub-carriers could be used at the cost of additional power. Similarly more FCW bits can be added to allow more frequencies, however a higher resolution bandwidth is required in the receiver to distinguish them. More ACW states could also be added however when difference in amplitude become too small, the required link SNR to determine their differences will become problematic. For our prototype link we use 8 different symbols in our "symbol library" (the list of permissible AFSK sub-carrier settings from which transmit symbols can be chosen) as shown in Fig. 3. Our symbol library was selected from the 512 permissible states based on ensuring they are visibly different enough to identify clearly during testing.

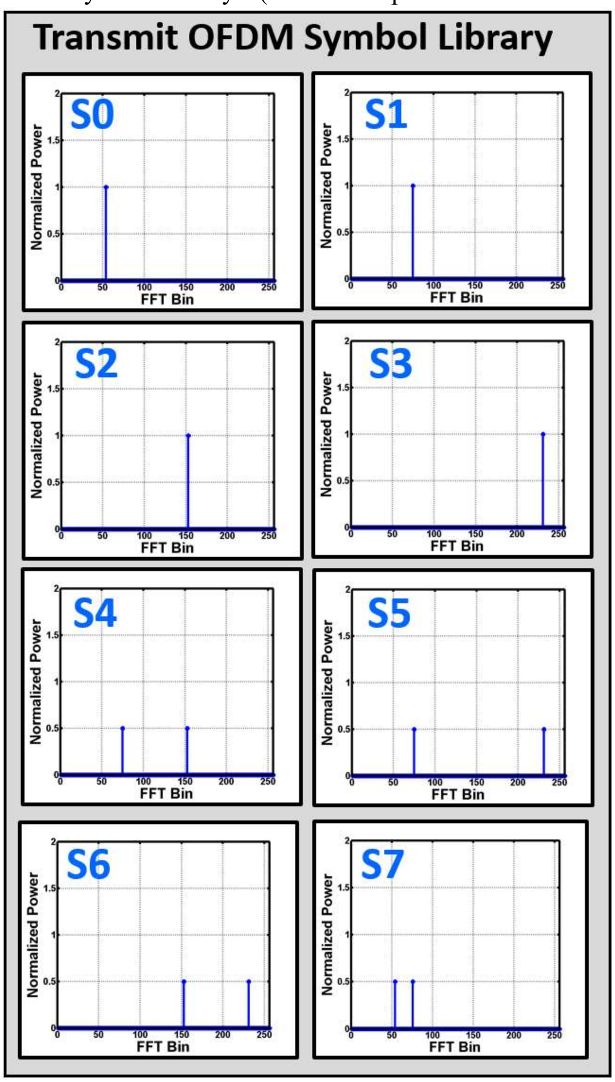

Fig. 3. Symbol library of 8 selectable AFSK sub-carrier states for data transmission (down-selected from 512 possible frequency-amplitude states).

Once the symbols are generated by the DDFS array, a set of R2R DACs are used to convert each digital sub-carrier to an analog format. The R2R DACs are chosen as the sample rate is not high (32 MHz) and the R values can be made large enough (20K in this design) to minimize the required DC power. As only 4 amplitude steps are used in the modulator linearity is not critical and a modest bit count is acceptable (8 in our demonstration). Finally each DAC drives a parallel reflection modulator which periodically applies a 50 ohm resistor to the antenna port of the backscatter transmitter to modulate the reflection coefficient with the associated sub-carrier. Again linearly of the modulator device is not critical as only 4 amplitude steps are used.

III. Link Demonstration

To demonstrate our DDFS based AFSK-ODFM backscatter modulator we constructed a 65nm CMOS chip containing a 4-parallel DDFS-DAC array as well as a 3-bit output pseudo-random bit sequence generator to generate transmit data as shown in Fig 4a. The chip is driven from an external 32 MHz clock, which is further divided by 8 to drive the prbs to provide a symbol rate is 4MS/s. Each time the PRBS is clocked the random 3-bit output is used to select one of the 8 symbols in the symbol library, which is then applied to the FCW/ACW input for each path of the DDFS/DAC array. The sub-carrier settings for each of the 8 library symbols are programmable through an SPI interface.

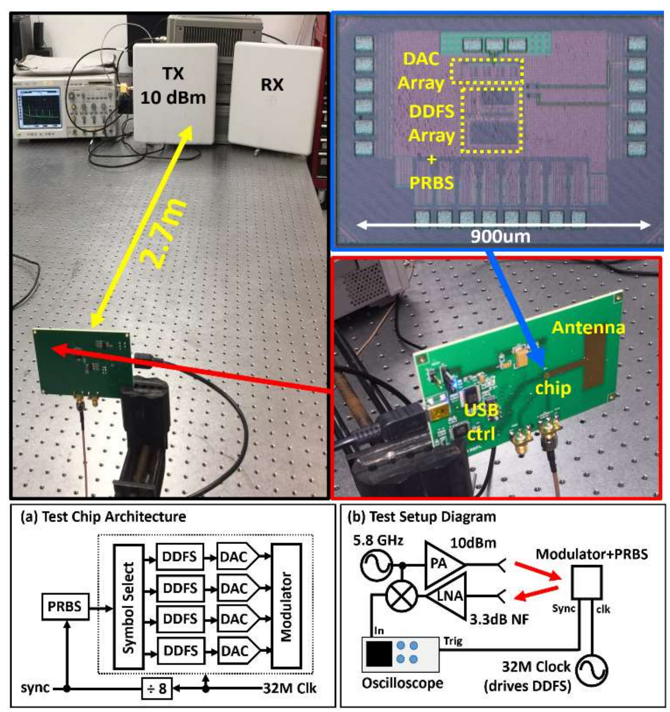

Fig. 4(a).Block diagram of test chip. (b) Setup diagram. (c) Photo of setup including Tx/Rx, chip die photo and test PCB.

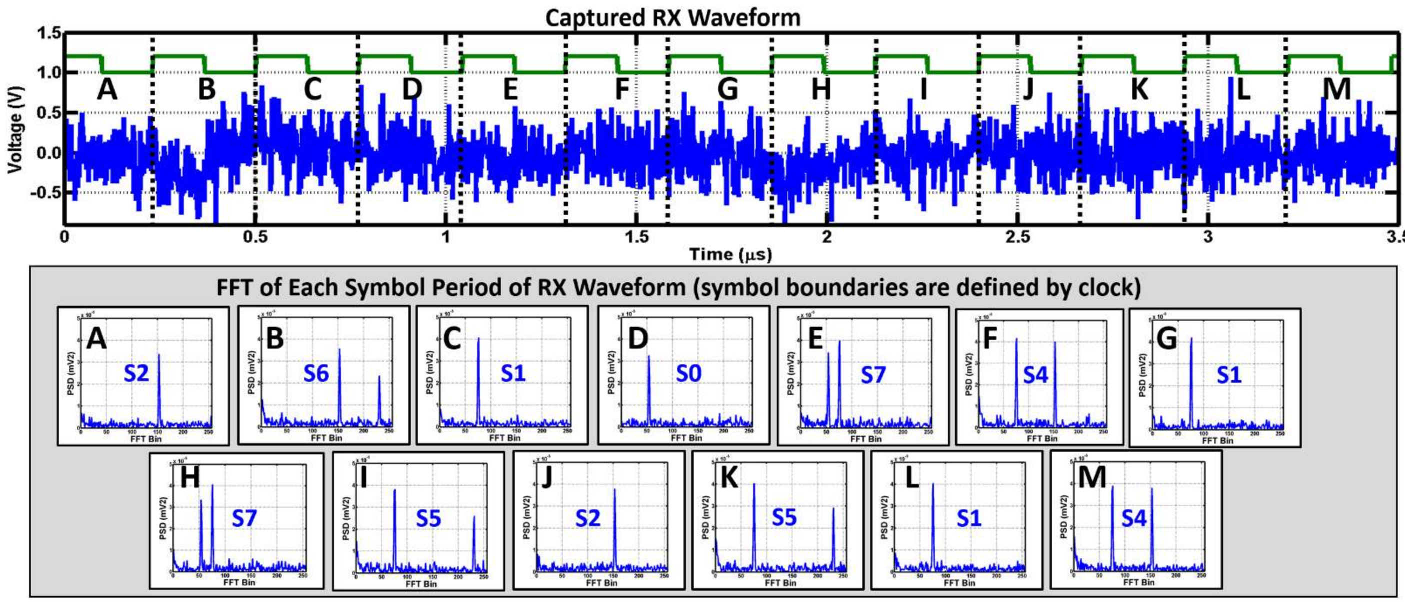

Fig. 5. Time domain signal captured from the base-station receiver and clock signal used to generate the transmit symbols. The FFT is taken with each symbol period defining the transform window, revealing the individual OFDM symbols inside as well as their corresponding name from the symbol library.

The 65nm CMOS chip was bonded to a PCB and introduced into the test setup shown in Fig. 4b where a 10 dBm base-station transmitter at 5.8 GHz shines of continuous-wave (CW) power while a receiver offering a 3.3 dB noise figure at 5.8 GHz monitors the reflection from the backscatter chip. The output of the receiver is captured on a time domain scope that is triggered with the 4 MHz clock from the transmitter's PRBS so to keep track of symbol boundaries (the time at which each symbol period starts and ends). In a fully deployed system this trigger would be replaced by a full clock/data recovery (CDR) system within the base-station receiver. The base-station and AFSK-OFDM backscatter transmitter were placed 2.7 m apart as shown in Fig. 4c. Commercial microwave antennas were used to implement the base-station transmitter and receiver, each offering 8dBi of directive gain. The received waveform at the base-station was captured and recorded on a digital time-domain oscilloscope along with the 4 MHz sync used to track the symbol period boundaries as shown in Fig 5. Using this captured time-domain sequence several symbol periods in length are imported into Mathworks Matlab environment to emulate the functions of an AFSK-OFDM demodulator. Within each symbol period, the receiver time-domain waveform is windowed and a PSD taken, revealing the individual OFDM symbols contained inside. After inspection it is obvious which symbol from the transmitter library each captured signal corresponds to.

To demonstrate this, we show the results of the PSD transform of the receiver output waveform for thirteen captured symbol periods labelled A-to-M in Fig. 5. For each period, we also list which transmitted library symbol matches the captured and transformed symbol. Slight changes in relative amplitude between various tones is created as the frequency response of the antennas and transceiver components used in the testing base-station have has some amplitude variation across their passband. The antenna used on the test-PCB also offered some amplitude variation across the 5.8 GHz band of interest.

VI. Conclusions

In this paper, we have introduced a backscatter transmitter architecture capable of correctly relaying AFSK-OFDM symbols to a base-station for low power IoT applications. The architecture uses DDFS-based sub-carrier generation to produce AFSK symbols that are then transformed to analog before transmission. A full free-space test of a complete backscatter link was performed confirming the AFSK-OFDM symbols are being correctly relayed to the base-station. The prototype transmitter was implemented in a 65nm CMOS technology where it occupies 0.45mm^2 and consumed 1.77mW during transmission.

Acknowledgement

The authors are grateful to TSMC for 65nm support. Part of this work was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

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